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**18EVE15**

## First Semester M.Tech. Degree Examination, Dec.2018/Jan.2019
## Digital VLSI Design

Time: 3 hrs.                                                                     Max. Marks: 100

**Note:** *Answer FIVE full questions, choosing*
*ONE full question from each module.*

### Module-1

1   a. Derive an expression for the drain current of enhancement n-channel MOSFET when operating in linear region, saturation region and when channel length is modulated.
**(08 Marks)**

    b. Draw the VTC of nMOS inverter with resistive load and derive an expression for the $V_{OH}$, $V_{OL}$, $V_{IL}$ and $V_{IH}$.
**(12 Marks)**

### OR

2   a. What is scaling? Describe two methods of scaling. Also justify which scaling method is good.
**(05 Marks)**

    b. Explain the concept of accumulation, depletion and inversion with corresponding energy band diagram.
**(10 Marks)**

    c. Find the noise margin of a resistive load inverter circuit with $V_{DD} = 5V$, $k_n' = 20\mu A/V^2$, $V_{To} = 0.8V$, $R_L = 200k\Omega$ and $W/L = 2$.
**(05 Marks)**

### Module-2

3   a. Draw the VTC of CMOS inverter and derive an expression for the $V_{OH}$, $V_{OL}$, $V_{IL}$ $V_{IH}$ and $V_{th}$.
**(10 Marks)**

    b. Draw the circuit diagram of CMOS inverter indicating all types of capacitances and write the expression for load capacitance.
**(04 Marks)**

    c. Derive an expression for the $\tau_{PHL}$ of CMOS inverter.
**(06 Marks)**

### OR

4   a. Find the noise margin and the switching threshold ($V_{th}$) of a CMOS inverter with $V_{DD} = 3.3V$, $V_{TO, n} = 0.6V$, $V_{TO,P} = -0.7V$, $\mu_n C_{ox} = 60\mu A/V^2$, $\mu_p C_{OX} = 16\mu A/V^2$, $(W/L)_n = 8$, and $(W/L)_P = 12$.
**(08 Marks)**

    b. Derive an expression for the Elmore delay of RC network.
**(06 Marks)**

    c. Derive an expression for the dynamic power consumption of the CMOS inverter.
**(06 Marks)**

### Module-3

5   a. Draw the detailed circuit diagram of 3-transistor DRAM and describe the read/write operation with timing diagram.
**(08 Marks)**

    b. Describe the organization of 4 M bit DRAM.
**(04 Marks)**

    c. Explain with diagram the NOR flash memory cell operation and NAND flash memory cell operation.
**(08 Marks)**

**OR**

6   a.  Draw the circuit diagram of SRAM cell with sense amplifier and read/write circuit and describe the operation with read and write timing diagram. **(08 Marks)**

b.  Draw the memory structure of FRAM cell array and describe the read timing diagram. **(08 Marks)**

c.  Draw the circuit diagram of NOR-based raw decoder circuit for 2-address bits and 4 word lines. **(04 Marks)**

## Module-4

7   a.  Describe the operation of pass transistor and derive an expression for logic '1' transfer and logic '0' transfer. **(08 Marks)**

b.  Derive the carry expression for the 4-bit CLA adder and implement the carry expressions by using multiple-output domino CMOS fute. **(06 Marks)**

c.  Realize the following Boolean expression using BiCMOS logic $f = \overline{ab(c + d + e)}$. **(06 Marks)**

**OR**

8   a.  Describe the working principle of voltage Bootstrapping. **(06 Marks)**

b.  Describe the dynamic behavior of BJT by deriving the corresponding expressions. **(10 Marks)**

c.  Draw the circuit diagram of a TSPC based rising edge triggered D-flip-flop and describe its operation and mention the advantages. **(04 Marks)**

## Module-5

9   a.  Describe the possible input and output circuits of VLSI chips. **(05 Marks)**

b.  Describe the process variation in output waveform of a 4-bit adder. **(05 Marks)**

c.  What is latch-up? Explain the concept of latch-up with neat diagram and suggest how latch-up can be avoided. **(10 Marks)**

**OR**

10  a.  Describe the various model of ESD testing. Also describe the various ESD protection circuit. **(10 Marks)**

b.  Describe circuit parameters, noise parameter distributions and circuit performance measures used in design for manufacturability. **(10 Marks)**

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